

# DATA SHEET

## **TZA3019** 2.5 Gbits/s dual postamplifier with level detectors and $2 \times 2$ switch

Product specification  
Supersedes data of 2000 Apr 10  
File under Integrated Circuits, IC19

2001 Jun 25

## 2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

# TZA3019

### FEATURES

- Dual postamplifier
- Single 3.3 V power supply
- Wideband operation from 50 kHz to 2.5 GHz (typical value)
- Fully differential
- Channels are delay matched
- On-chip DC-offset compensations without external capacitor
- Interfacing with positive or negative supplied logic
- Switching possibility between channels
- Positive Emitter Coupled Logic (PECL) or Current-Mode Logic (CML) compatible data outputs adjustable from 200 to 800 mV (p-p) single-ended
- Power-down capability for unused outputs and detectors
- Rise and fall times 80 ps (typical value)
- Possibility to invert the output of each channel separately
- Input level-detection circuits for Received Signal Strength Indicator (RSSI) or Loss Of Signal (LOS) detection, programmable from 0.4 to 400 mV (p-p) single-ended, with open-drain comparator output for direct interfacing with positive or negative logic
- Reference voltage for output level and LOS adjustment
- Automatic strongest input signal switch possibility (TZA3019 version B)
- HTQFP32 or HBCC32 plastic package with exposed pad.

### APPLICATIONS

- Postamplifier for Synchronous Digital Hierarchy and Synchronous Optical Network (SDH/SONET) transponder
- SDH/SONET wavelength converter
- Crosspoint or channel switch
- PECL driver
- Fibre channel arbitrated loop
- Protection ring
- Monitoring
- Signal level detectors
- Swing converter CML 200 mV (p-p) to PECL 800 mV (p-p)
- Port bypass circuit
- 2.5 GHz clock amplification.

### GENERAL DESCRIPTION

The TZA3019 is a low gain postamplifier multiplexer with a dual RSSI and/or LOS detector that is designed for use in critical signal path control applications, such as loop-through, redundant channel switching or Wavelength Division Multiplexing (WDM). The signal path is unregistered, so no clock is required for the data inputs. The signal path is fully differential and delay matched. It is capable of operating from 50 kHz to 2.5 GHz.

The TZA3019 HTQFP32 and HBCC32 packages can be delivered in three versions:

- TZA3019AHT and TZA3019AVH with two RSSI signals
- TZA3019BHT and TZA3019BVH with one RSSI and one LOS signal
- TZA3019CHT and TZA3019CVH with two LOS signals.

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TZA3019AHT	HTQFP32	plastic, heatsink thin quad flat package; 32 leads; body 5 × 5 × 1.0 mm	SOT547-2
TZA3019BHT	HTQFP32	plastic, heatsink thin quad flat package; 32 leads; body 5 × 5 × 1.0 mm	SOT547-2
TZA3019CHT	HTQFP32	plastic, heatsink thin quad flat package; 32 leads; body 5 × 5 × 1.0 mm	SOT547-2
TZA3019AVH	HBCC32	plastic, heatsink bottom chip carrier; 32 terminals; body 5 × 5 × 0.65 mm	SOT560-1
TZA3019BVH	HBCC32	plastic, heatsink bottom chip carrier; 32 terminals; body 5 × 5 × 0.65 mm	SOT560-1
TZA3019CVH	HBCC32	plastic, heatsink bottom chip carrier; 32 terminals; body 5 × 5 × 0.65 mm	SOT560-1
TZA3019U	–	bare die; 2.22 × 2.22 × 0.28 mm	–

# 2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

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## BLOCK DIAGRAM

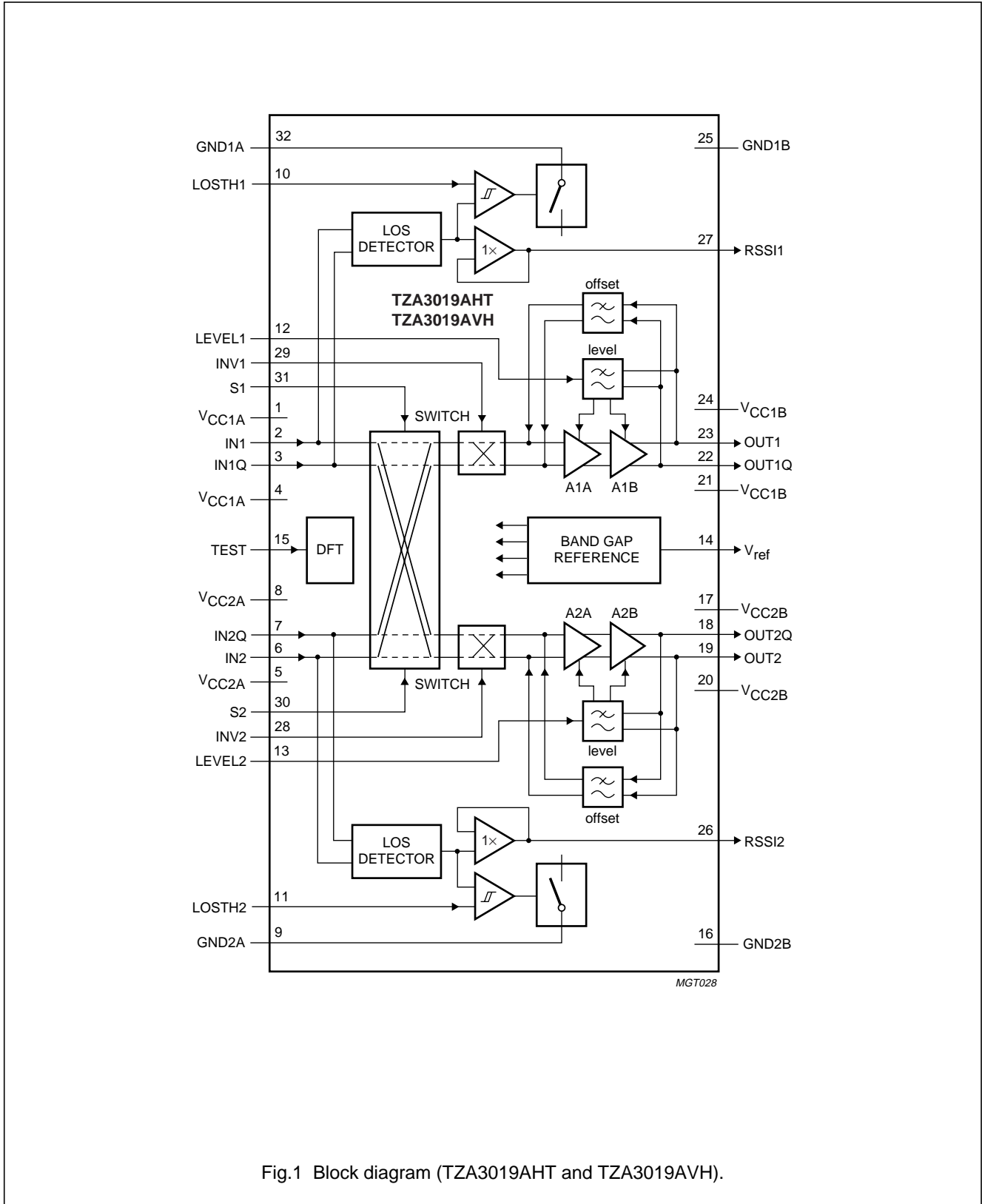


Fig.1 Block diagram (TZA3019AHT and TZA3019AVH).

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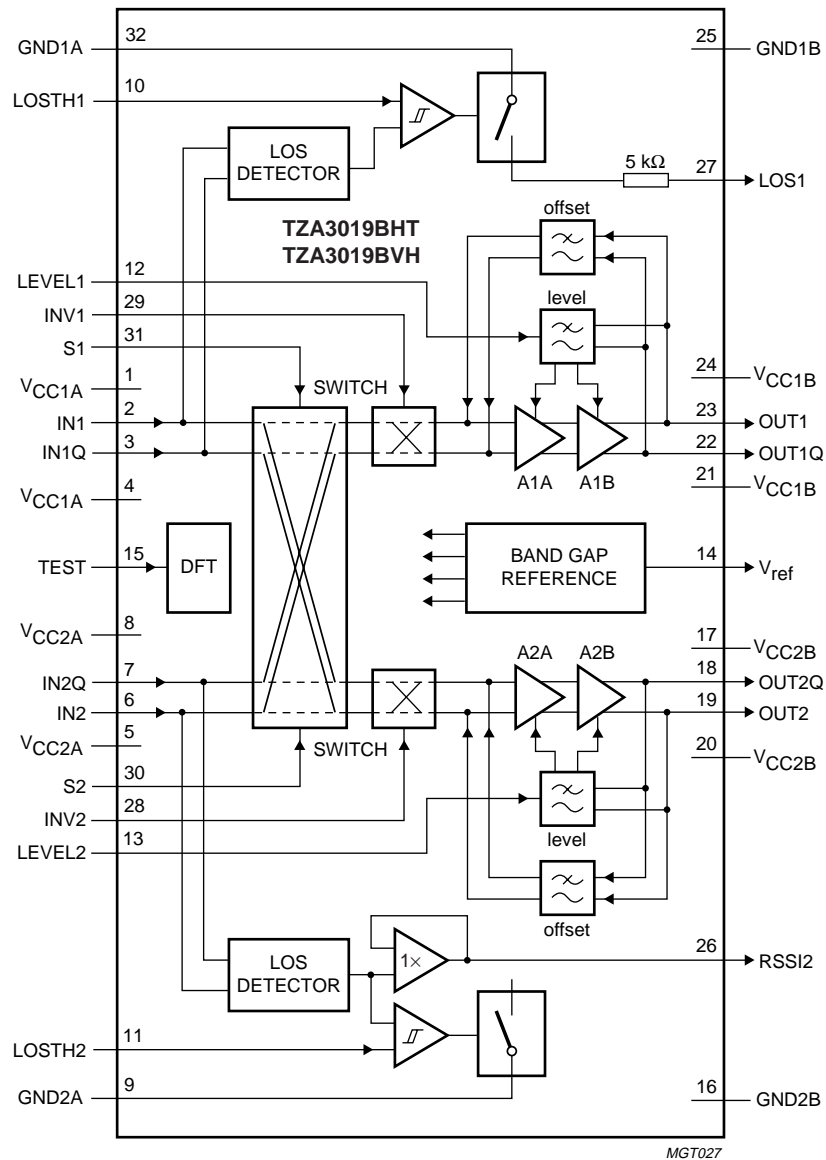


Fig.2 Block diagram (TZA3019BHT and TZA3019BVH).

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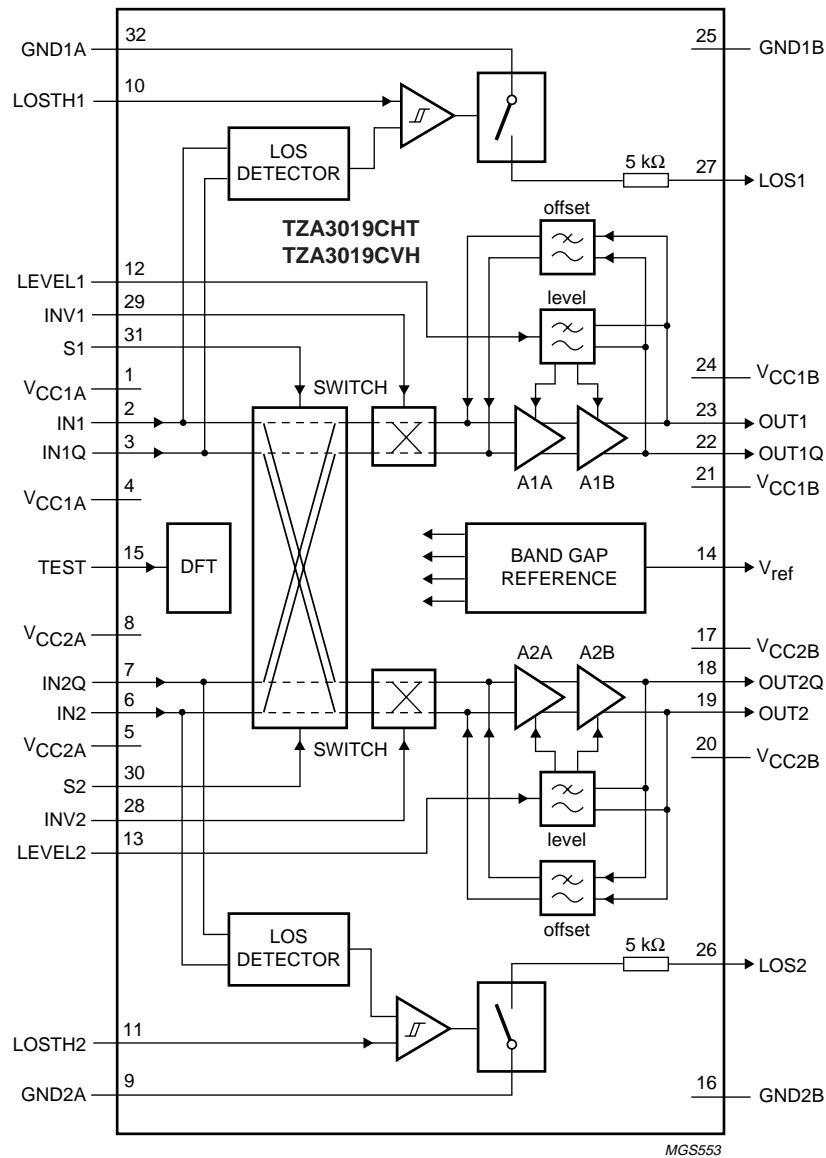


Fig.3 Block diagram (TZA3019CHT and TZA3019CVH).

## 2.5 Gbits/s dual postamplifier with level detectors and $2 \times 2$ switch

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### PINNING

SYMBOL	PIN			PAD	TYPE <sup>(2)</sup>	DESCRIPTION
	TZA3019xHT/xVH <sup>(1)</sup>					
	A	B	C			
V <sub>CC1A</sub>	1	1	1	1	S	supply voltage for input 1 and LOS1 circuits
IN1	2	2	2	2	I	differential circuit 1 input; complimentary to pin IN1Q; DC bias level is set internally at approximately $V_{CC} - 0.33$ V
IN1Q	3	3	3	3	I	differential circuit 1 input; complimentary to pin IN1; DC bias level is set internally at approximately $V_{CC} - 0.33$ V
V <sub>CC1A</sub>	4	4	4	4	S	supply voltage for input 1 and LOS1 circuits
n.c.	–	–	–	5	–	not connected
n.c.	–	–	–	6	–	not connected
V <sub>CC2A</sub>	5	5	5	7	S	supply voltage for input 2 and LOS2 circuits
IN2	6	6	6	8	I	differential circuit 2 input; complimentary to pin IN2Q; DC bias level is set internally at approximately $V_{CC} - 0.33$ V
IN2Q	7	7	7	9	I	differential circuit 2 input; complimentary to pin IN2; DC bias level is set internally at approximately $V_{CC} - 0.33$ V
V <sub>CC2A</sub>	8	8	8	10	S	supply voltage for input 2 and LOS2 circuits
GND2A	9	9	9	11	S	ground for input 2 and LOS2 circuits
LOSTH1	10	10	10	12	I	input for level detector programming of input 1 circuit; threshold level is set by connecting external resistors between pins V <sub>CC1A</sub> and V <sub>ref</sub> ; when forced to GND1A or not connected, the LOS1 circuit will be switched off
LOSTH2	11	11	11	13	I	input for level detector programming of input 2 circuit; threshold level is set by connecting external resistors between pins V <sub>CC2A</sub> and V <sub>ref</sub> ; when forced to GND2A or not connected, the LOS2 circuit will be switched off
n.c.	–	–	–	14	–	not connected
LEVEL1	12	12	12	15	I	input for programming output level of output 1 circuit; output level is set by connecting external resistors between pins V <sub>CC1A</sub> and V <sub>ref</sub> ; when forced to V <sub>CC1A</sub> or not connected, pins OUT1 and OUT1Q will be switched off
LEVEL2	13	13	13	16	I	input for programming output level of output 2 circuit; output level is set by connecting external resistors between pins V <sub>CC2A</sub> and V <sub>ref</sub> ; when forced to V <sub>CC2A</sub> or not connected, pins OUT2 and OUT2Q will be switched off
V <sub>ref</sub>	14	14	14	17	O	reference voltage for level circuit and LOS threshold programming; typical value is $V_{CC} - 1.6$ V; no external capacitor allowed
n.c.	–	–	–	18	–	not connected
TEST	15	15	15	19	I	for test purposes only; to be left open-circuit in the application
GND2B	16	16	16	20	S	ground for output 2 circuit
V <sub>CC2B</sub>	17	17	17	21	S	supply voltage for output 2 circuit
OUT2Q	18	18	18	22	O	PECL or CML compatible differential circuit 2 output; complimentary to pin OUT2

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SYMBOL	PIN			PAD	TYPE <sup>(2)</sup>	DESCRIPTION
	TZA3019xHT/xVH <sup>(1)</sup>					
	A	B	C			
OUT2	19	19	19	23	O	PECL or CML compatible differential circuit 2 output; complimentary to pin OUT2Q
V <sub>CC2B</sub>	20	20	20	24	S	supply voltage for output 2 circuit
n.c.	–	–	–	25	–	not connected
n.c.	–	–	–	26	–	not connected
V <sub>CC1B</sub>	21	21	21	27	S	supply voltage for output 1 circuit
OUT1Q	22	22	22	28	O	PECL or CML compatible differential circuit 1 output; complimentary to pin OUT1
OUT1	23	23	23	29	O	PECL or CML compatible differential circuit 1 output; complimentary to pin OUT1Q
V <sub>CC1B</sub>	24	24	24	30	S	supply voltage for output 1 circuit
GND1B	25	25	25	31	S	ground for output 1 circuit
RSSI2	26	26	–	32	O	output of received signal strength indicator of detector 2
LOS2	–	–	26	33	O-DRN	output loss of signal detector 2; detection of input 2 signal; direct drive of positive or negative supplied logic via internal 5 kΩ resistor
RSSI1	27	–	–	34	O	output of received signal strength indicator of detector 1
LOS1	–	27	27	35	O-DRN	output loss of signal detector 1; detection of input 1 signal; direct drive of positive or negative supplied logic via internal 5 kΩ resistor
INV2	28	28	28	36	TTL	input to invert the signal of pins OUT2 and OUT2Q; directly positive (inverted) or negative supplied logic driven
INV1	29	29	29	37	TTL	input to invert the signal of pins OUT1 and OUT1Q; directly of positive (inverted) or negative supplied logic driven
S2	30	30	30	38	TTL	input selector output 2 circuit; directly positive (inverted) or negative supplied logic driven
S1	31	31	31	39	TTL	input selector output 1 circuit; directly positive (inverted) or negative supplied logic driven
GND1A	32	32	32	40	S	ground for input 1 and LOS1 circuits
GNDp	pad	pad	pad	–	S	ground pad (exposed die pad)

### Notes

1. The 'x' in TZA3019xHT/xVH represents versions A, B and C.
2. Pin type abbreviations: O = output, I = input, S = power supply, TTL = logic input and O-DRN = open-drain output.

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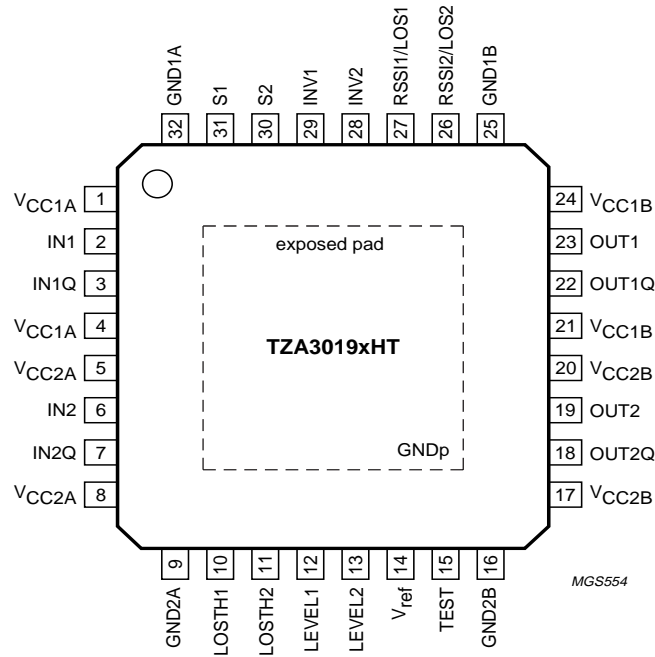


Fig.4 Pin configuration HTQFP32 package.

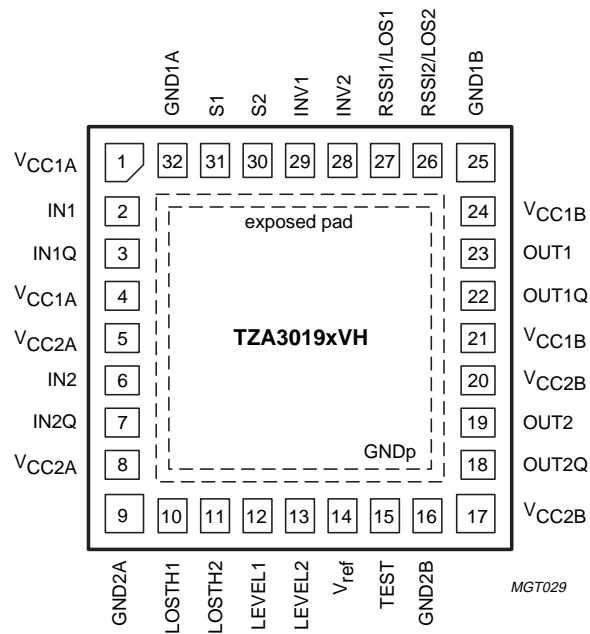


Fig.5 Pin configuration HBCC32 package.



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### FUNCTIONAL DESCRIPTION

The TZA3019 is a dual postamplifier with multiplexer and loss of signal detection (see Figs 1, 2 and 3). The RF path starts with the multiplexer, which connects an amplifier to one of the two inputs. It is possible to invert the output for easy layout of the Printed-Circuit Board (PCB). The signal is amplified to a certain level. To guarantee this level with minimum distortion over the temperature range and level range, an active control part is added. The offset compensation circuit following the inverter minimizes the offset.

The Received Signal Strength Indicator (RSSI) or the Loss Of Signal (LOS) detector uses a 7-stage 'successive detection' circuit. It provides a logarithmic output. The LOS detector is followed by a comparator with a programmable threshold. The input signal level-detection is implemented to check if the input signal voltage is above the user programmed level. This can insure that data will only be transmitted when the input signal-to-noise ratio is sufficient for low bit error rate system operation. A second offset compensation circuit minimizes the offset of the logarithmic amplifier.

### RF input circuit

The input circuit contains internal  $50 \Omega$  resistors decoupled to  $V_{CC}$  via an internal common mode  $12 \text{ pF}$  capacitor (see Fig.6).

The input pins are DC-biased at approximately  $V_{CC} - 0.33 \text{ V}$  by an internal reference generator. The TZA3019 can be DC-coupled, but AC-coupling is preferred. In case of DC-coupling, the driving source must operate within the allowable input range ( $V_{CC} - 1.0 \text{ V}$  to  $V_{CC} + 0.3 \text{ V}$ ). A DC-offset voltage of more than a few millivolts should be avoided, since the internal DC-offset compensation circuit has a limited correction range. When AC-coupling is used, if no DC-compatibility is required, the values of the coupling capacitors must be large enough to pass the lowest input frequency of interest. Capacitor tolerance and resistor variation must be included for an accurate calculation. Do not use signal frequencies around the low cut-off circuit frequencies ( $f_{-3\text{dB}(l)} = 50 \text{ kHz}$  for the postamplifiers and  $f_{-3\text{dB}(l)} = 1 \text{ MHz}$  for the LOS circuits).

### RF output circuit

Matching the main amplifier outputs (see Fig.7) is not mandatory. In most applications, the transmission line receiving end will be properly matched, while very little reflections occur.

Matching the transmitting end to absorb reflections is only recommended for very sensitive applications.

In such cases, pull-up resistors of  $100 \Omega$  should be connected as close as possible to the IC from pins OUT1 and OUT1Q, and pins OUT2 and OUT2Q to GND1B and GND2B respectively. These matching resistors are not needed in most applications.

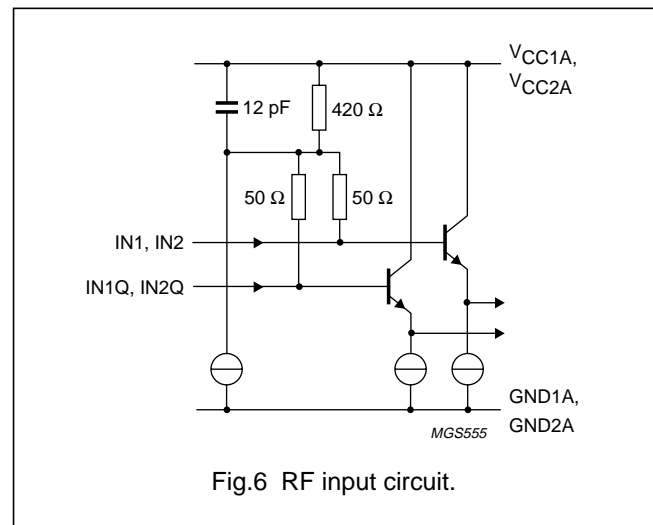


Fig.6 RF input circuit.

### Postamplifier level adjustment

The postamplifier boosts the signal up to PECL levels. The output can be either CML- or PECL-level compatible, adjusted by means of the voltage on pins LEVEL1 and LEVEL2. The DC voltages of pins OUT1 and OUT1Q, and pins OUT2 and OUT2Q match with the DC-levels on pins LEVEL1 and LEVEL2, respectively. Due to the receiving end  $50 \Omega$  load resistance, it means that at the same level of  $V_{o(p-p)}$ ,  $V_{\text{LEVEL1}}$  and  $V_{\text{LEVEL2}}$  with AC-coupling are not equal to  $V_{\text{LEVEL1}}$  and  $V_{\text{LEVEL2}}$  with DC-coupling (see Figs 7 and 8).

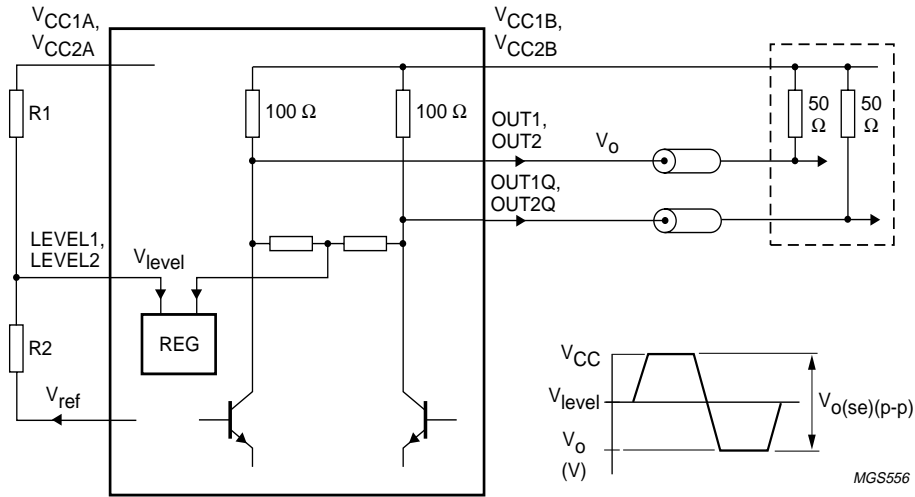
When pin LEVEL1 or LEVEL2 is connected to  $V_{CC}$  or not connected, the postamplifier is in power-down state (see Fig.7).

### Postamplifier DC offset cancellation loop

Offset control loops connected between the inputs of the buffers A1A and A2A and the outputs of the amplifiers A1B and A2B (see Figs 1, 2 and 3) will keep the input of both buffers at their toggle point during the absence of an input signal. The active offset compensation circuit is integrated, so no external capacitor is required. The loop time constant determines the lower cut-off frequency of the amplifier chain. The cut-off frequency of the offset compensations is fixed internally at approximately  $5 \text{ kHz}$ .

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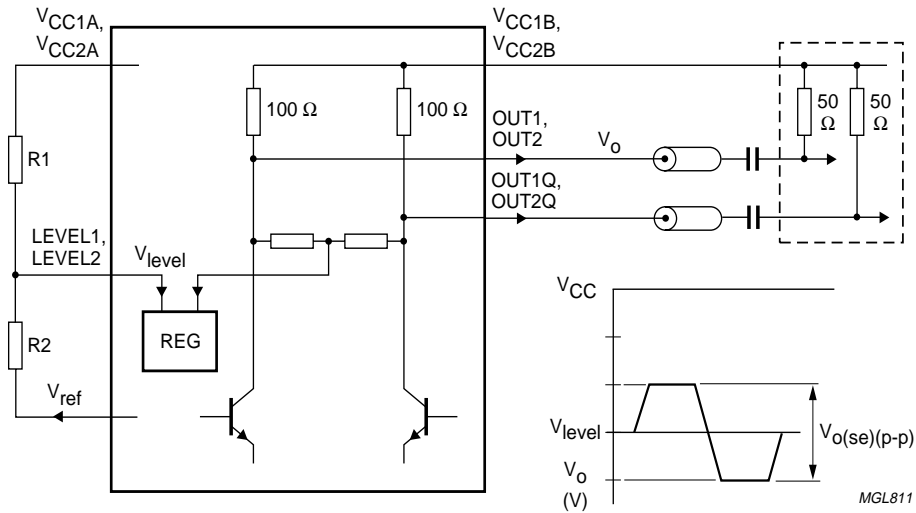


$$V_{level} = 0.5 \times V_{o(se)(p-p)}$$

$$V_{level} = V_{ref} \times \frac{R1}{R1 + R2}$$

Level detector in power-down mode:  $V_{LEVEL1}$  or  $V_{LEVEL2} = V_{CC}$ .

a. DC-coupling.



$$V_{level} = 1.5 \times V_{o(se)(p-p)}$$

$$V_{level} = V_{ref} \times \frac{R1}{R1 + R2}$$

Level detector in power-down mode:  $V_{LEVEL1}$  or  $V_{LEVEL2} = V_{CC}$ .

b. AC-coupling.

Fig.7 RF output configurations.

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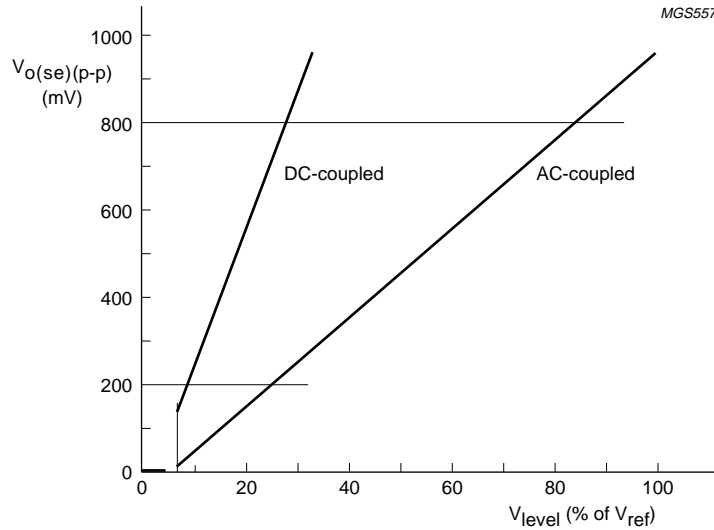


Fig.8 Output signal as a function of  $V_{level}$ .

**TTL logic input of selector and inverter**

The logic levels are differently defined for positive or negative logic (see Fig.9). It should be noted that positive logic levels are inverted if a negative supply voltage is used.

**Outputs as a function of switch input pins S1, S2, INV1 and INV2**

See Tables 1, 2, 3 and 4.

The default value for the switch input pins S1, S2, INV1 and INV2 if not connected, is zero.

**Table 1** OUT1 and OUT1Q as function of input S1

S1	OUT1	OUT1Q
0	IN1	IN1Q
1	IN2	IN2Q

**Table 2** OUT2 and OUT2Q as function of input S2

S2	OUT2	OUT2Q
0	IN2	IN2Q
1	IN1	IN1Q

**Table 3** OUT1 and OUT1Q as function of input INV1

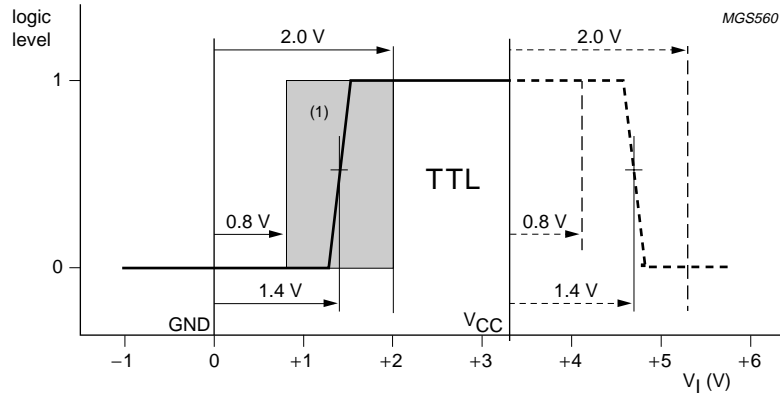
INV1	OUT1	OUT1Q
0	IN1 or IN2	IN1Q or IN2Q
1	IN1Q or IN2Q	IN1 or IN2

**Table 4** OUT2 and OUT2Q as function of input INV2

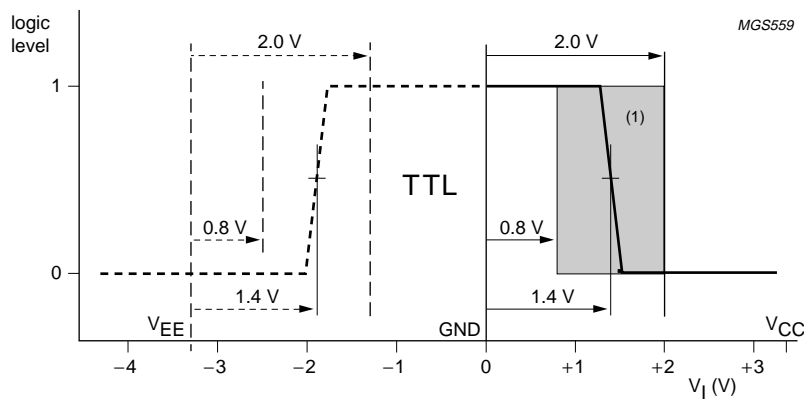
INV2	OUT2	OUT2Q
0	IN1 or IN2	IN1Q or IN2Q
1	IN1Q or IN2Q	IN1 or IN2

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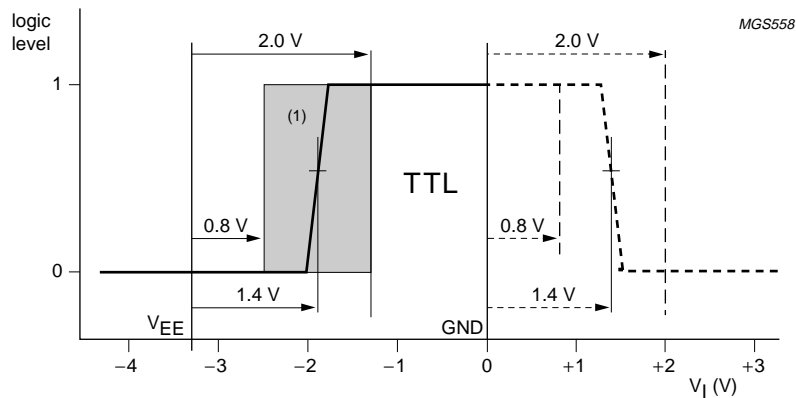
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a. Positive circuit supply voltage  $V_{CC}$  and positive logic supply voltage  $V_{CC}$ .



b. Negative circuit supply voltage  $V_{EE}$  and positive logic supply voltage  $V_{CC}$ .



c. Negative circuit supply voltage  $V_{EE}$  and positive logic supply voltage  $V_{EE}$ .

(1) Level not defined.

Fig.9 Logic levels on pins S1, S2, INV1 and INV2 as a function of the input voltages.

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### RSSI and LOS detection

The TZA3019 allows AC-signal level detection. This can prevent the outputs from reacting to noise during the absence of a valid input signal, and can insure that data only will be transmitted when the signal-to-noise ratio of the input signal is sufficient to insure low bit error rate system operation.

The RSSI detection circuit uses seven limiting amplifiers in a ‘successive detection’ topology to closely approximate logarithmic response over a total range of 70 dB. The detectors provide full-wave rectification of the AC signals presented at each previous amplifier stage. Their outputs are current drivers. Each cell incorporates a low-pass filter, being the first step in recovering the average value of the demodulated signal of the input frequency. The summed detector output currents are converted to a voltage by an internal load resistor. This voltage is buffered and available in the A and B versions of the TZA3019. When  $V_{RSSI}$  is used  $V_{LOSTH}$  must not be connected to GND to prevent the LOS comparator from switching to the standby mode. The LOS comparator detects an input signal above a fixed threshold, resulting in a LOW-level at the LOS circuit output. The threshold level is determined by the voltage on pins LOSTH1 or LOSTH2 (see Fig.10). A filter with a time constant of 1  $\mu$ s nominal is included to prevent noise spikes from triggering the level detector.

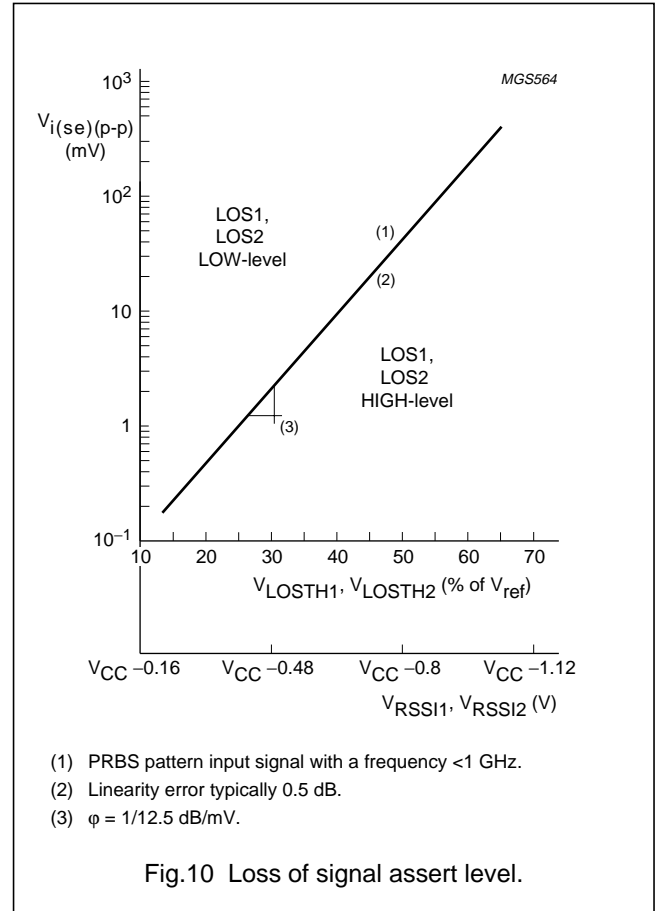
The comparator (with internal 3 dB hysteresis) drives an open-drain circuit with an internal resistor (5 k $\Omega$ ) for direct interfacing to positive or negative logic (see Fig.11). Only available in the B and C versions of the TZA3019.

The response is independent of the sign of the input signal because of the particular way the circuit has been built. This is part of the demodulating nature of the detector, which results in an alternating input voltage being transformed to a rectified and filtered quasi DC-output signal. For the TZA3019 the logarithmic voltage slope is  $\phi = 1/12.5$  dB/mV and is essentially temperature and supply independent through four feedback loops in the reference circuit. The internal LOS detector output voltage is based on  $V_{ref}$ . The demodulator characteristic depends on the waveform and the response depends roughly on the input signal RMS value. This influences high frequencies, a square wave input of 2.4 GHz (LOS circuit bandwidth of 2.4 GHz) offsets the intercept voltage by 20%.  $V_{LOSTH}$  can be calculated using the following formula:

$$V_{LOSTH} = V_{RSSI} = V_{CC} + 0.458 - S_{RSSI} \times 20 \log \left( \frac{V_{i(p-p)}}{26E - 8} \right) \quad (1)$$

where  $S_{RSSI}$  = sensitivity (see Chapter “Characteristics”).

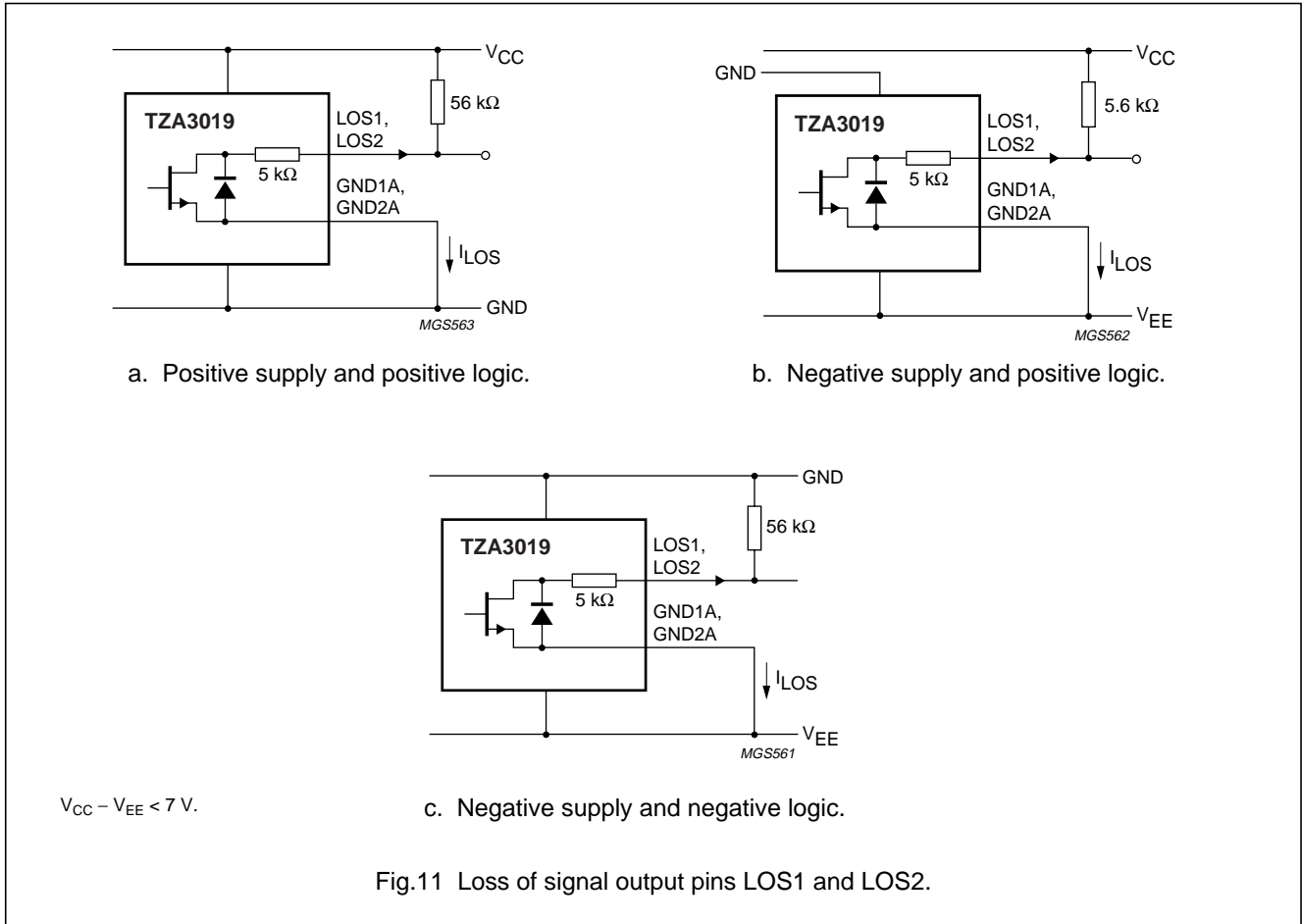
Example: a 200 mV (p-p) single-ended 1.2 GB/s PRBS signal has an  $V_{RSSI}$  of  $V_{CC} - 1.013$  V.



A full understanding of the offset control loop is useful. The primary purpose of the loop is to extend the lower end of the dynamic range in any case where the offset voltage of the first stage might be high enough to cause later stages to prematurely enter limiting, caused by the high DC-gain of the amplifier system. The offset is automatically and continuously compensated via a feedback path from the last stage. An offset at the output of the logarithmic converter is equivalent to a change of amplitude at the input. Consequently, with DC-coupling, signal absence, either LOW-level or HIGH-level is detected as a full signal, only signals with an average value equal to zero give zero output. Version B can be used for an auto function, which switches the strongest input signal to output 1 and the weakest to output 2. To achieve this output  $V_{RSSI2}$  must be used as the reference voltage for input  $V_{LOSTH}$ . Then the output LOS1 can switch S1 and S2.

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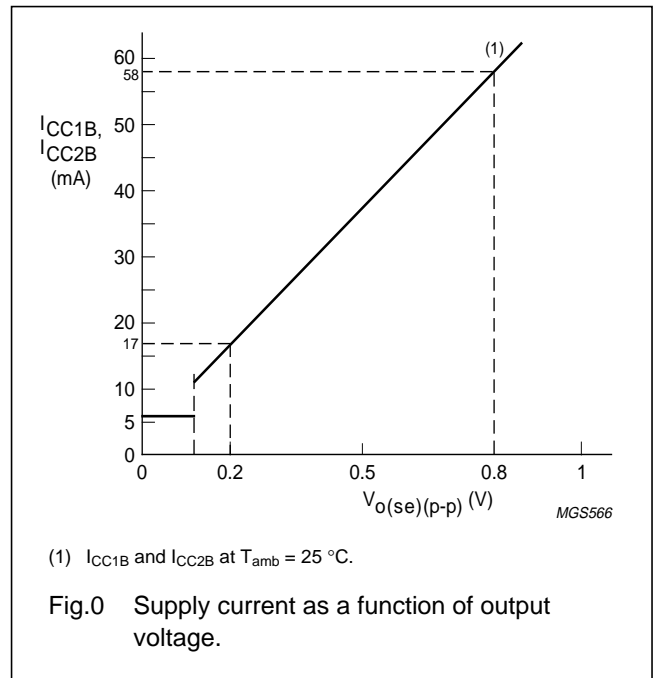


### Supply current

For the supply currents  $I_{CC1B}$  and  $I_{CC2B}$ , see Fig.0.

#### Using a positive supply voltage

Although the TZA3019 has been designed to use a single +3.3 V supply voltage (see Fig.13), some care should be taken with respect to RF transmission lines. The on-chip signals refer to the various  $V_{CC}$  pins. The external transmission lines will most likely be referred to the pins  $V_{GND1A}$ ,  $V_{GND2A}$ ,  $V_{GND1B}$  and  $V_{GND2B}$ , being the system ground. The RF signals will change from one reference plane to another when interfacing the RF inputs and outputs. A positive supply application is very vulnerable to interference with respect to this point. For a successful +3.3 V application, special care should be taken when designing the PCB layout in order to reduce the influence of interference and to keep the positive supply voltage as clean as possible.



## 2.5 Gbits/s dual postamplifier with level detectors and $2 \times 2$ switch

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### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage	-0.5	+5.5	V
$V_n$	DC voltage			
	pins IN1, IN1Q, IN2, IN2Q, LOSTH1, LOSTH2, LEVEL1, LEVEL2, $V_{ref}$ , TEST, OUT2Q, OUT2, OUT1Q, OUT1, GNDp, $V_{CC1A}$ , $V_{CC2A}$ , $V_{CC1B}$ and $V_{CC2B}$	-0.5	$V_{CC} + 0.5$	V
	pins LOS1, LOS2, INV1, INV2, S1 and S2	-0.5	+7	V
$I_n$	DC current			
	pins IN1, IN1Q, IN2 and IN2Q	-20	+20	mA
	pins LOSTH1, LOSTH2, LEVEL1 and LEVEL2	0	14	$\mu$ A
	pins $V_{ref}$ , TEST, LOS1 and LOS2	-1	+1	mA
	pins OUT1, OUT1Q, OUT2 and OUT2Q	-30	+30	mA
	pins INV1, INV2, S1 and S2	0	20	$\mu$ A
$P_{tot}$	total power dissipation	-	1.2	W
$T_{stg}$	storage temperature	-65	+150	$^{\circ}$ C
$T_j$	junction temperature	-	150	$^{\circ}$ C
$T_{amb}$	ambient temperature	-40	+85	$^{\circ}$ C

### THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point (exposed die pad)	note 1	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	1s2p multi-layer test board; notes 1 and 2	33	K/W
$R_{th(s-a)}$	thermal resistance from solder point to ambient (exposed die pad)	1s2p multi-layer test board; notes 1 and 2	18	K/W
$R_{th(s-a)(req)}$	required thermal resistance from solder point to ambient	LOS circuits switched on		
		$V_o = 200$ mV (p-p) single-ended; both output circuits	60	K/W
		$V_o = 800$ mV (p-p) single-ended; both output circuits	30	K/W

#### Notes

- JEDEC standard.
- HTQFP32 and HBCC32 packages.

## 2.5 Gbits/s dual postamplifier with level detectors and $2 \times 2$ switch

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### CHARACTERISTICS

Typical values at  $T_{amb} = 25\text{ °C}$  and  $V_{CC} = 3.3\text{ V}$ ; minimum and maximum values are valid over the entire ambient temperature range and supply voltage range; all voltages referenced to ground; note 1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supply</b>						
SUPPLY PINS $V_{CC1A}$ , $V_{CC1B}$ , $V_{CC2A}$ AND $V_{CC2B}$						
$V_{CC}$	supply voltage		3.13	3.3	3.47	V
$I_{CC1A}$ , $I_{CC2A}$	supply current A	LOS circuit power-down	14	24	34	mA
		LOS circuit switched on	24	40	56	mA
$I_{CC1B}$ , $I_{CC2B}$	supply current B	amplifier power-down	2	6	10	mA
		$V_o = 200\text{ mV (p-p)}$ single-ended; one output circuit	11	17	24	mA
		$V_o = 800\text{ mV (p-p)}$ single-ended; one output circuit	43	60	77	mA
$P_{tot}$	total power dissipation	power-down	100	200	300	mW
		both LOS circuits switched on $V_o = 200\text{ mV (p-p)}$ single-ended; both output circuits	220	380	555	mW
		$V_o = 800\text{ mV (p-p)}$ single-ended; both output circuits	450	660	925	mW
TC	temperature coefficient	LOS circuit switched on; $I_{CC1A}$ ; $I_{CC2A}$	-80	-50	-30	$\mu\text{A/K}$
		$V_o = 800\text{ mV (p-p)}$ single-ended; $I_{CC1B}$ ; $I_{CC2B}$	-50	-30	-15	$\mu\text{A/K}$
$T_j$	junction temperature		-40	-	+125	$^{\circ}\text{C}$
$T_{amb}$	ambient temperature		-40	+25	+85	$^{\circ}\text{C}$
<b>Inputs multiplexer and loss of signal detector</b>						
PECL OR CML INPUT PINS IN1, IN1Q, IN2 AND IN2Q						
$V_{i(p-p)}$	input voltage swing (peak-to-peak value)	single-ended; notes 2 and 3	50	-	500	mV
$V_{i(bias)}$	DC input bias voltage		$V_{CC} - 0.4$	$V_{CC} - 0.33$	$V_{CC} - 0.28$	V
$V_i$	DC and AC input window voltage	note 3	$V_{CC} - 1.0$	-	$V_{CC} + 0.3$	V
$R_i$	input resistance	single-ended	35	50	70	$\Omega$
$C_i$	input capacitance	single-ended; note 3	0.6	0.8	1.2	pF



## 2.5 Gbits/s dual postamplifier with level detectors and $2 \times 2$ switch

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Postamplifier</b>						
AMPLIFIERS A1A, A1B, A2A AND A2B						
$G_v$	small signal voltage gain	$V_o = 200$ mV (p-p) single-ended; note 4	9	15	20	dB
		$V_o = 800$ mV (p-p) single-ended; note 4	21	29	34	dB
$f_D$	signal path data rate	notes 5 and 9	–	2.5	–	Gbits/s
$f_{-3dB(l)}$	low –3 dB cut-off frequency DC compensation	note 3	2	5	10	kHz
$f_{-3dB(h)}$	high –3 dB cut-off frequency		–	2.0	–	GHz
$t_{PD}$	propagation delay	note 3	150	200	250	ps
$\Delta t_{PD}$	propagation delay difference	at the same signal levels; note 3	–	0	5	ps
J	total jitter	20 bits of the 28.5 kbits pattern; notes 3 and 6	–	8	–	ps
$\alpha_{ct}$	crosstalk	crosstalk of IC only	–	110	–	dB
PECL OR CML OUTPUT PINS OUT1, OUT1Q, OUT2 AND OUT2Q						
$V_{o(se)(p-p)}$	single-ended output voltage (peak-to-peak value)	50 $\Omega$ load	200	–	800	mV
TC	temperature coefficient output level		–1	0	+1	mV/K
$t_r$	rise time	20% to 80%; notes 5 and 6	–	80	–	ps
$t_f$	fall time	80% to 20%; notes 5 and 6	–	80	–	ps
$R_o$	output resistance	single-ended	70	100	130	$\Omega$
$C_o$	output capacitance	single-ended; note 3	0.6	0.8	1.2	pF
LEVEL CONTROL INPUT PINS LEVEL1 AND LEVEL2						
$V_i$	input voltage		$V_{CC} - V_{ref}$	–	$V_{CC}$	V
$R_i$	input resistance	measured to $V_{CC1A}$ or $V_{CC2A}$	150	350	600	k $\Omega$
<b>Multiplexer and inverter switch</b>						
PECL OR CML INPUT PINS IN1, IN1Q, IN2 AND IN2Q						
$\alpha_{OS(red)}$	input offset reduction	$V_o = 200$ mV (p-p) single-ended; note 7	3.8	9	13.5	dB
		$V_o = 800$ mV (p-p) single-ended; note 7	6	14	22	dB
$V_{io(cor)}$	input offset voltage correction range	peak-to-peak value; single-ended	–10	–	+10	mV
$V_{n(i)(eq)(rms)}$	equivalent input noise voltage (RMS value)	$V_o = 800$ mV (p-p) single-ended; note 3	–	75	170	$\mu$ V
$F_n$	noise factor	note 3	–	5	12	dB

## 2.5 Gbits/s dual postamplifier with level detectors and $2 \times 2$ switch

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>SWITCH CIRCUIT</b>						
$t_a$	assert time	multiplexer and inverter	–	100	–	ns
$t_d$	de-assert time	multiplexer and inverter	–	80	–	ns
<b>TTL INPUT PINS S1, S2, INV1 AND INV2</b>						
$V_{IL}$	LOW-level input voltage	positive logic; note 10	–0.3	–	+0.8	V
$V_{IH}$	HIGH-level input voltage	positive logic; note 10	2.0	–	$V_{CC} + 0.8$	V
$R_i$	input resistance	measured to GND1A or GND2A	100	180	400	k $\Omega$
$I_i$	input current		–40	–	+40	$\mu$ A
<b>Received signal strength indicator and loss of signal detector</b>						
<b>RSSI AND LOS CIRCUIT</b>						
$V_{i(se)(p-p)}$	single-ended input voltage swing (peak-to-peak value)		0.4	–	400	mV
DR	dynamic range		57	60	63	dB
$S_{RSSI}$	LOS sensitivity	50 MHz, square; note 8	10	12.5	15	mV/dB
		620 MHz, square; note 8	10	12	14	mV/dB
		1.2 GHz, square; note 8	9	11	13.5	mV/dB
		100 MB/s PRBS ( $2^{31} - 1$ ); note 8	9	12.5	15	mV/dB
		1.2 GB/s PRBS ( $2^{31} - 1$ ); note 8	10	12	14.5	mV/dB
		2.4 GB/s PRBS ( $2^{31} - 1$ ); note 8	10	12	14	mV/dB
$TC_{sens}$	temperature coefficient sensitivity		–2	0	+2	$\mu$ V/dBK
LE	linearity error	see Fig.10; note 3	–	0.5	1	dB
$\alpha_{OS(red)}$	input offset reduction	notes 3 and 7	25	35	50	dB
$V_{io(cor)}$	on-chip DC-offset compensation correction range	peak-to-peak value single-ended	–5	–	+5	mV
$f_{-3dB(l)}$	low –3 dB cut-off frequency		0.5	1	2	MHz
$f_{-3dB(h)}$	high –3 dB cut-off frequency	note 8	1.5	2	2.5	GHz
<b>LOS CIRCUIT</b>						
$hy_{LOS}$	LOS hysteresis	input signal waveform dependency	2.0	3.0	4.0	dB
$t_a$	assert time	note 3	–	–	5	$\mu$ s
$t_d$	de-assert time	note 3	–	–	5	$\mu$ s

## 2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INPUT PINS LOSTH1 AND LOSTH2						
$V_i$	input voltage		0	–	$V_{CC}$	V
$R_i$	input resistance	measured to GND1A or GND2A	150	350	600	k $\Omega$
OUTPUT PINS LOS1 AND LOS2						
$I_{o(sink)}$	output sink current		–	–	1	mA
$R_o$	output resistance	internal output series resistance	3.5	5	6.5	k $\Omega$
OUTPUT PINS RSSI1 AND RSSI2						
$V_o$	output voltage		$V_{CC} - 1.2$	–	$V_{CC}$	V
$I_o$	output current		–1	–	+1	mA
<b>Band gap reference circuit</b>						
OUTPUT PIN $V_{ref}$						
$V_{ref}$	reference voltage		$V_{CC} - 1.85$	$V_{CC} - 1.6$	$V_{CC} - 1.45$	V
$C_{ext}$	allowed external capacitance		–	–	10	pF
$I_{o(sink)}$	output sink current		–	–	500	$\mu$ A

### Notes

- It is assumed that both CML inputs carry a complementary signal with the specified peak-to-peak value (true differential excitation).
- Minimum signal with limiting output.
- Guaranteed by design.
- $G_V = \frac{V_o}{V_i}$
- Based on –3dB cut-off frequency.
- $V_i = 100$  mV (p-p) single-ended and  $V_o = 200$  mV (p-p) single-ended.
- Input offset reduction =  $\frac{G_{AC}}{G_{DC}}$
- Sensitivity depends on the waveform and is therefore a function of –3 dB cut-off frequency see Equation (1).
- Low limit can go as low as DC if input signal overrides input offset voltage correction range.
- When using a negative supply voltage, positive or negative logic can be used. The values will be different (see Fig.9).

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## 2.5 Gbits/s dual postamplifier with level detectors and $2 \times 2$ switch

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TZA3019

### APPLICATION INFORMATION

#### RF input and output connections

Striplines, or microstrips, with an odd mode characteristic impedance of  $Z_0 = 50 \Omega$  have to be used for the differential RF connections on the PCB. This applies to both the signal inputs and the signal outputs. The two lines in each pair should have the same length.

#### Grounding and power supply decoupling

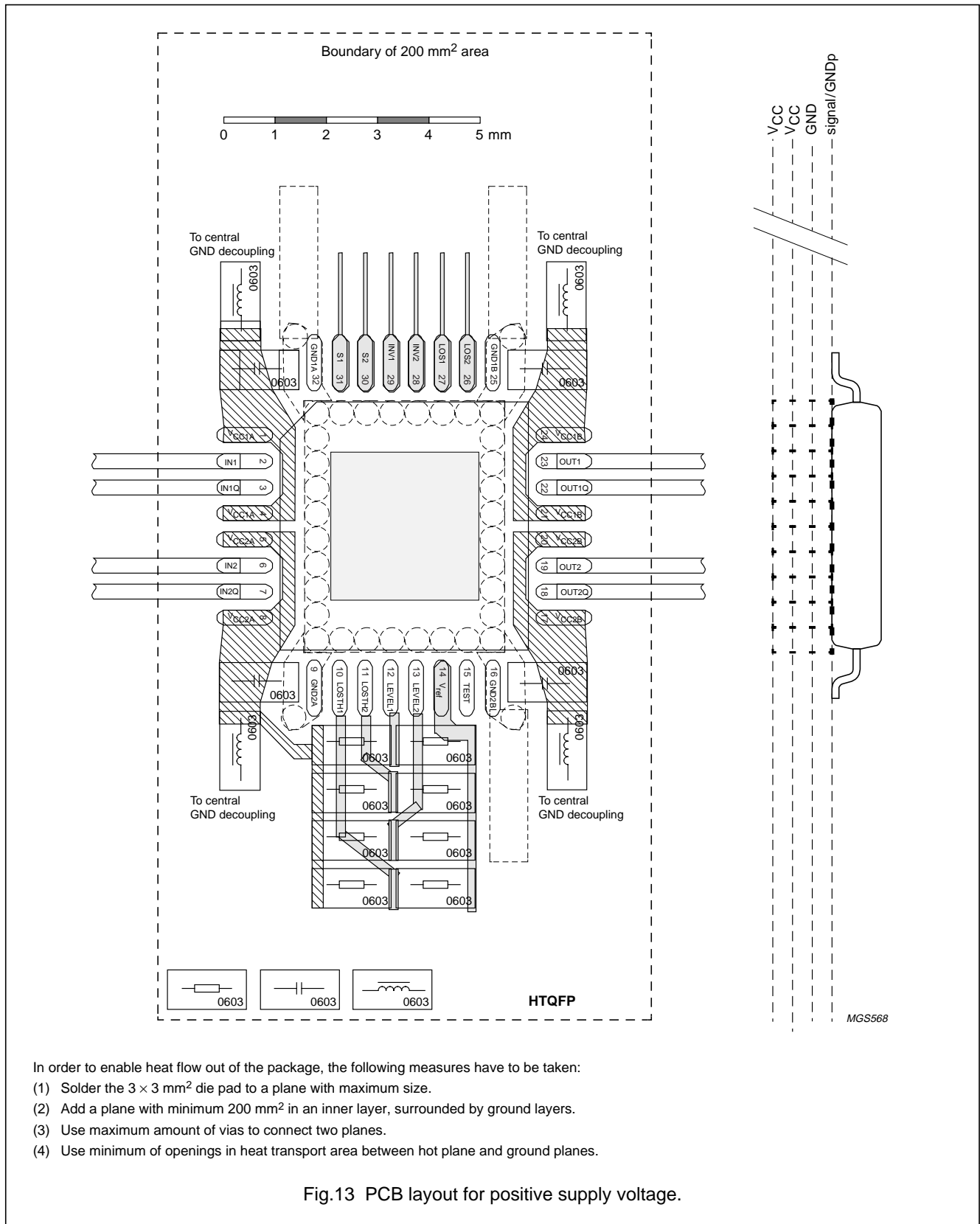
The ground connection on the PCB needs to be a large copper filled area connected to a common ground plane with an inductance as low as possible.

To minimize low frequency switching noise in the vicinity of the TZA3019, the power supply line should be filtered once using a beaded capacitor circuit with a low cut-off frequency.

The exposed die pad GNDp connection on the PCB also needs to be a large copper area to improve heat transfer to the PCB and thus support IC cooling (see Figs 13 and 14).

# 2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

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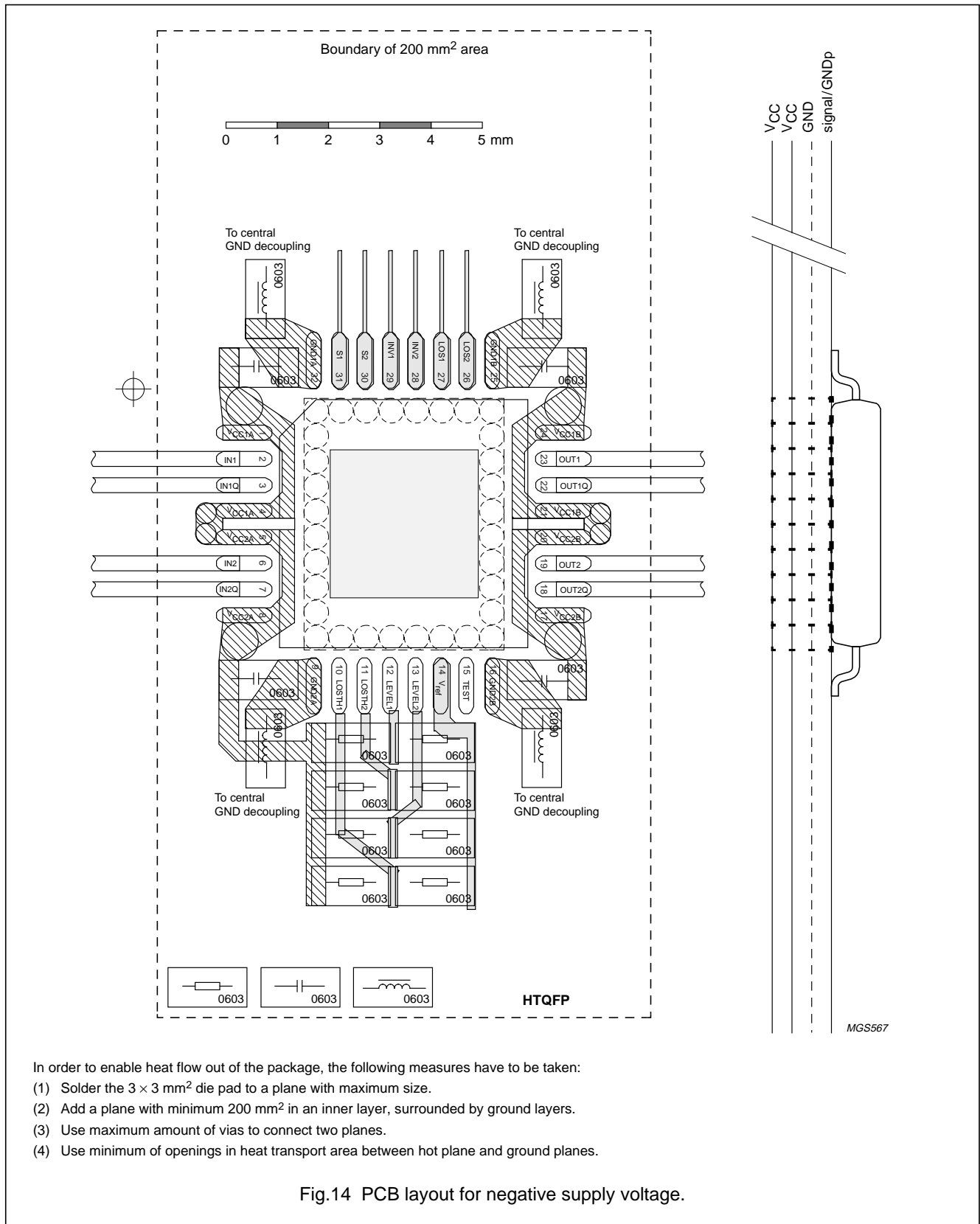
In order to enable heat flow out of the package, the following measures have to be taken:

- (1) Solder the 3 × 3 mm<sup>2</sup> die pad to a plane with maximum size.
- (2) Add a plane with minimum 200 mm<sup>2</sup> in an inner layer, surrounded by ground layers.
- (3) Use maximum amount of vias to connect two planes.
- (4) Use minimum of openings in heat transport area between hot plane and ground planes.

Fig.13 PCB layout for positive supply voltage.

# 2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

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In order to enable heat flow out of the package, the following measures have to be taken:

- (1) Solder the 3 × 3 mm<sup>2</sup> die pad to a plane with maximum size.
- (2) Add a plane with minimum 200 mm<sup>2</sup> in an inner layer, surrounded by ground layers.
- (3) Use maximum amount of vias to connect two planes.
- (4) Use minimum of openings in heat transport area between hot plane and ground planes.

Fig.14 PCB layout for negative supply voltage.

## 2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

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### BONDING PAD LOCATIONS

SYMBOL	PAD	COORDINATES <sup>(1)</sup>	
		x	y
V <sub>CC1A</sub>	1	-928	+710
IN1	2	-928	+553
IN1Q	3	-928	+396
V <sub>CC1A</sub>	4	-928	+239
n.c.	5	-928	+81
n.c.	6	-928	-81
V <sub>CC2A</sub>	7	-928	-239
IN2	8	-928	-396
IN2Q	9	-928	-553
V <sub>CC2A</sub>	10	-928	-710
GND2A	11	-707	-928
LOSTH1	12	-550	-928
LOSTH2	13	-393	-928
n.c.	14	-236	-928
LEVEL1	15	-79	-928
LEVEL2	16	+79	-928
V <sub>ref</sub>	17	+236	-928
n.c.	18	+393	-928
TEST	19	+550	-928
GND2B	20	+707	-928
V <sub>CC2B</sub>	21	+928	-710
OUT2Q	22	+928	-553

SYMBOL	PAD	COORDINATES <sup>(1)</sup>	
		x	y
OUT2	23	+928	-396
V <sub>CC2B</sub>	24	+928	-239
n.c.	25	+928	-81
n.c.	26	+928	+81
V <sub>CC1B</sub>	27	+928	+239
OUT1Q	28	+928	+396
OUT1	29	+928	+553
V <sub>CC1B</sub>	30	+928	+710
GND1B	31	+707	+928
RSSI2	32	+550	+928
LOS2	33	+393	+928
RSSI1	34	+236	+928
LOS1	35	+79	+928
INV2	36	-79	+928
INV1	37	-236	+928
S2	38	-393	+928
S1	39	-550	+928
GND1A	40	-707	+928

#### Note

- All x and y coordinates represent the position of the centre of the pad in  $\mu\text{m}$  with respect to the centre of the die (see Fig.15).

2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

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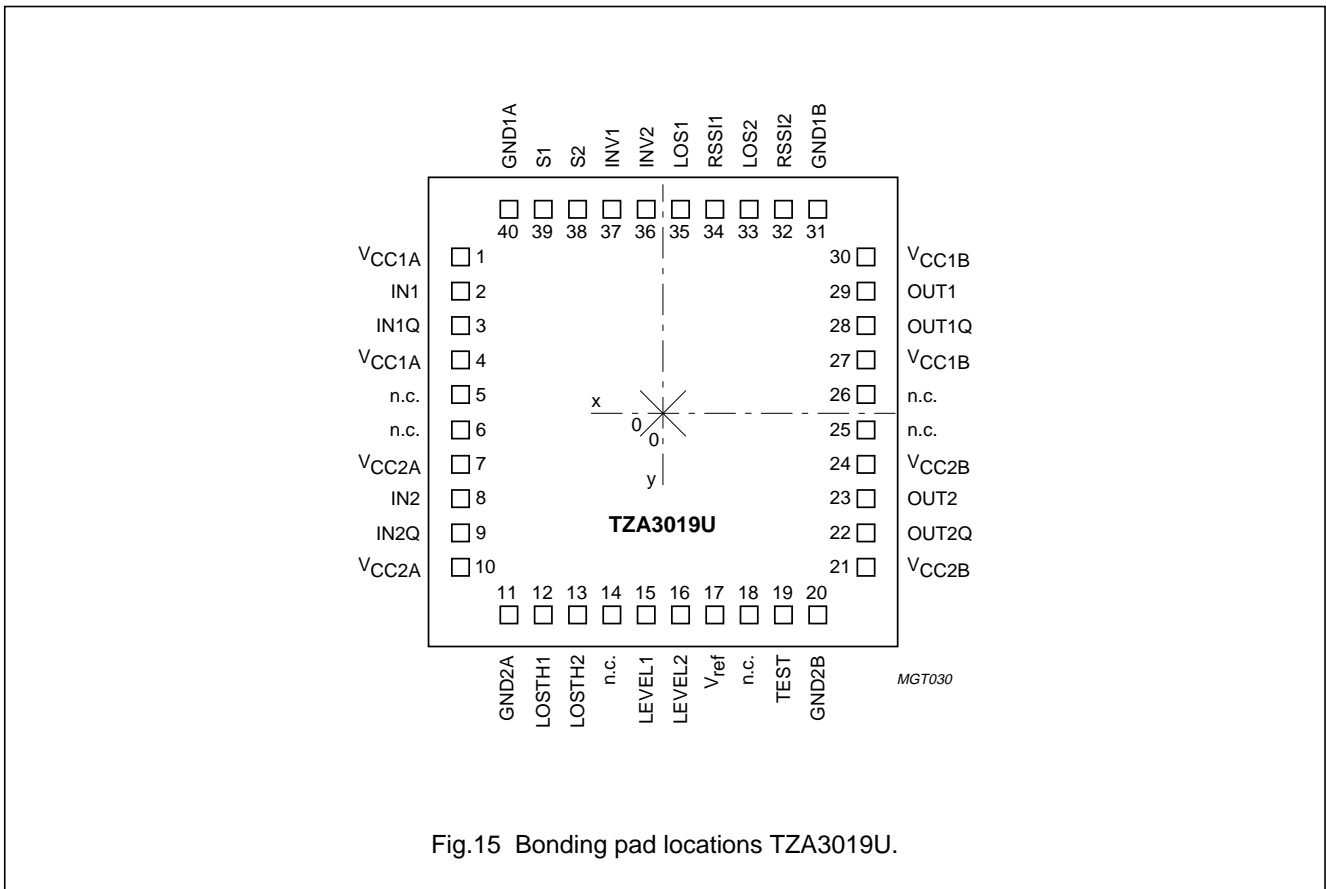


Fig.15 Bonding pad locations TZA3019U.



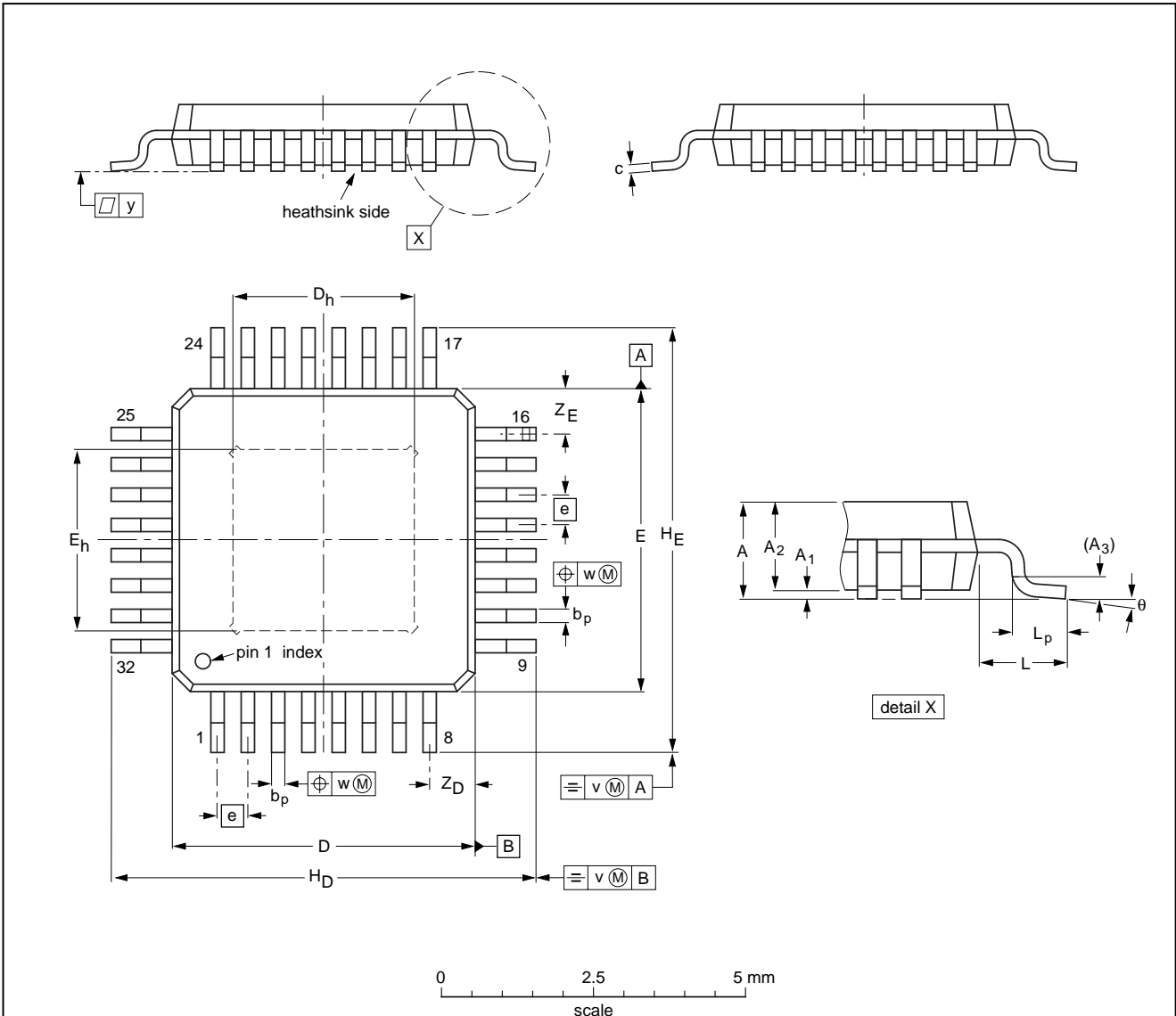
# 2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

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## PACKAGE OUTLINES

HTQFP32: plastic, heatsink thin quad flat package; 32 leads; body 5 x 5 x 1.0 mm

SOT547-2



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	D <sub>h</sub>	E <sup>(1)</sup>	E <sub>h</sub>	e	H <sub>D</sub>	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sub>D</sub> <sup>(1)</sup>	Z <sub>E</sub> <sup>(1)</sup>	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.20 0.09	5.1 4.9	3.1 2.7	5.1 4.9	3.1 2.7	0.5	7.1 6.9	7.1 6.9	1.0	0.75 0.45	0.2	0.08	0.08	0.89 0.61	0.89 0.61	7° 0°

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

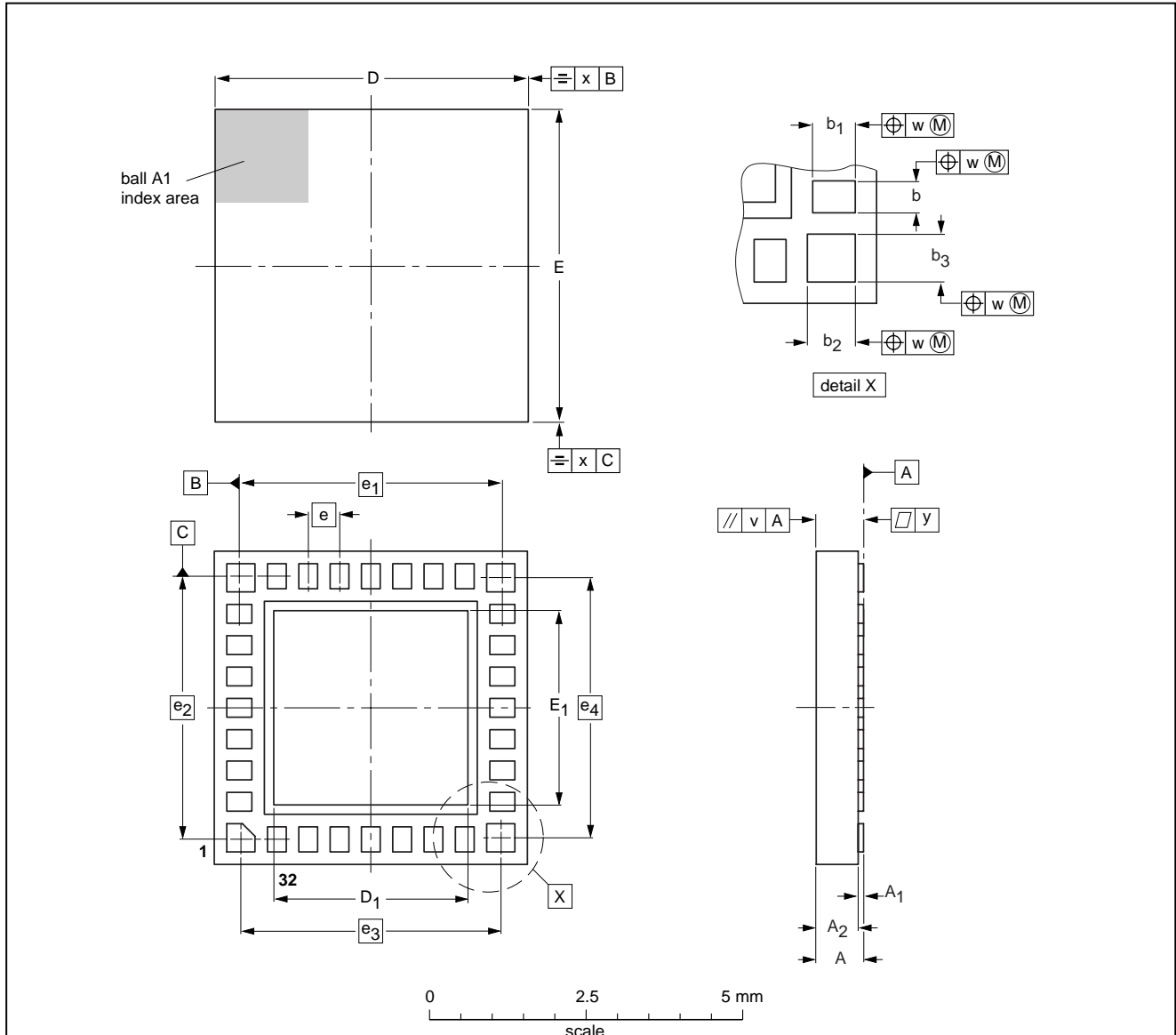
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT547-2						99-06-15

2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

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HBCC32: plastic, heatsink bottom chip carrier; 32 terminals; body 5 x 5 x 0.65 mm

SOT560-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	b	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	D	D <sub>1</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	e <sub>2</sub>	e <sub>3</sub>	e <sub>4</sub>	v	w	x	y
mm	0.80	0.10 0.05	0.70 0.60	0.35 0.20	0.50 0.30	0.50 0.35	0.50 0.35	5.1 4.9	3.2 3.0	5.1 4.9	3.2 3.0	0.5	4.2	4.2	4.15	4.15	0.2	0.15	0.15	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT560-1		MO-217				99-09-10 00-02-01

## 2.5 Gbits/s dual postamplifier with level detectors and $2 \times 2$ switch

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### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## 2.5 Gbits/s dual postamplifier with level detectors and 2 × 2 switch

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### Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW <sup>(1)</sup>
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable <sup>(2)</sup>	suitable
PLCC <sup>(3)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(3)(4)</sup>	suitable
SSOP, TSSOP, VSO	not recommended <sup>(5)</sup>	suitable

#### Notes

- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods".
- These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

#### DATA SHEET STATUS

DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)</sup>	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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#### Notes

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- The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

## 2.5 Gbits/s dual postamplifier with level detectors and $2 \times 2$ switch

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### DEFINITIONS

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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2.5 Gbits/s dual postamplifier with level  
detectors and 2 × 2 switch

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**NOTES**

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2.5 Gbits/s dual postamplifier with level  
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**NOTES**

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